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Terms	Documents
L2 and (network same port)	1

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DB=USPT,USOC; PLUR=YES; OP=OR			
L3	L2 and (network same port)	1	L3
L2	L1 and ((storage or memory) near5 serial$2)	15	L2
L1	((high adj1 speed) near5 bus) near10 (chipset or chip or IC or (integrtaed adj1 circuit))	204	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
L3	0

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Search: L5

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Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L5	L3	0	L5
L4	L3	0	L4
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	L2 and (network same port)	1	L3
L2	L1 and ((storage or memory) near5 serial$2)	15	L2
L1	((high adj1 speed) near5 bus) near10 (chipset or chip or IC or (integrtaed adj1 circuit))	204	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L2 same (high adj1 speed adj1 bus)	52

Database:

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US Patents Full-Text Database
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EPO Abstracts Database
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Search: L3

Refine Search

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DATE: Friday, June 25, 2004 Printable Copy Create Case

Set Name side by side	**Query**	**Hit Count**	**Set Name** result set
	DB=USPT,USOC; PLUR=YES; OP=OR		
L3	L2 same (high adj1 speed adj1 bus)	52	L3
L2	(high adj1 speed) same (storage or memory) same serial$2	5624	L2
	DB=USPT; PLUR=YES; OP=OR		
L1	5970069.pn. and (serial$2 near5 (disk or memory))	1	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L3	0

Database:

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Search: L4

Refine Search

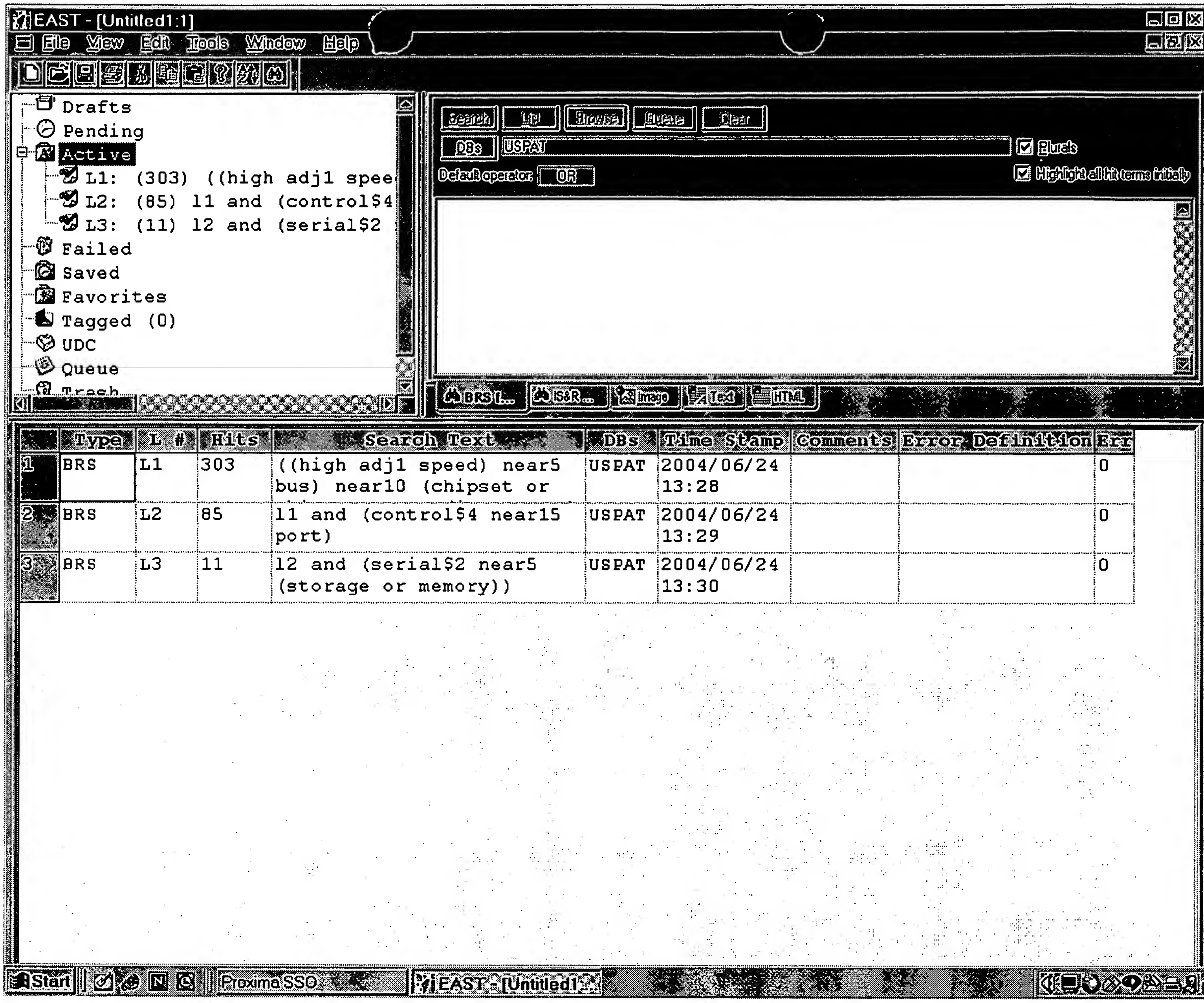
Recall Text Clear Interrupt

Search History

DATE: Friday, June 25, 2004 Printable Copy Create Case

Set Name side by side	**Query**	**Hit Count**	**Set Name** result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	L2 same (high adj1 speed adj1 bus)	52	L3
L2	(high adj1 speed) same (storage or memory) same serial$2	5624	L2
DB=USPT; PLUR=YES; OP=OR			
L1	5970069.pn. and (serial$2 near5 (disk or memory))	1	L1

END OF SEARCH HISTORY



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	303	((high adj1 speed) near5 bus) near10 (chipset or	USPAT	2004/06/24 13:28			0
2	BRS	L2	85	l1 and (control$4 near15 port)	USPAT	2004/06/24 13:29			0
3	BRS	L3	11	l2 and (serial$2 near5 (storage or memory))	USPAT	2004/06/24 13:30			0

EAST - [Untitled1:1]

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  - L2: (85) l1 and (control$4
  - L3: (11) l2 and (serial$2
- Failed
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DBs: USPAT

Plurals

Default operator: OR

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l2 and (serial$2 near5 (storage or memory))

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6633994 B1	20031014	11	Method and system for optimizing data transfers	713/600	710/306; 713/501
2	☐	☐	US 6584516 B1	20030624	12	High-speed servo data interface system	710/33	360/77.08; 710/7
3	☐	☐	US 6363510 B1	20020326	21	Electronic system for testing chips having a	714/738	324/158.1; 324/765;
4	☐	☐	US 6320711 B1	20011120	10	High-speed unified data interface for a read channel	360/46	360/41; 360/77.08
5	☐	☐	US 6317819 B1	20011113	71	Digital signal processor containing scalar processor	712/22	711/147; 712/10;
6	☐	☐	US 6163814 A	20001219	12	High speed servo data interface system for	710/1	360/77.08; 710/33
7	☐	☐	US 6037738 A	20000314	33	Servo control method and servo control system	318/625	318/560
8	☐	☐	US 5970069 A	19991019	103	Single chip remote access processor	370/402	370/401; 370/466
9	☐	☐	US 5646651 A	19970708	6	Block mode, multiple access multi-media/graphics memory	345/519	345/536; 345/546
10	☐	☐	US 5517626 A	19960514	150	Open high speed bus for microcomputer system	710/110	710/105; 711/118
11	☐	☐	US 4907225 A	19900306	62	Data protocol controller	370/463	

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1 **Beam position monitor data acquisition for the Advanced Photon So**
Lenkszus, F.R.; Kahana, E.; Votaw, A.J.; Decker, G.A.; Youngjoo Chung; Ciar D.J.; Laird, R.J.;
Particle Accelerator Conference, 1993., Proceedings of the 1993 , 17-20 May
Pages:1814 - 1816 vol.3

[Abstract] [PDF Full-Text (280 KB)] **IEEE CNF**

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2 **A low cost, high speed portable communications device: a case stuc using IDT RV4640 microprocessor & IDT77903 ATM card**
Kakkar, S.; Hussain, A.B.;
Compcon '97. Proceedings, IEEE , 23-26 Feb. 1997
Pages:172

[Abstract] [PDF Full-Text (32 KB)] **IEEE CNF**

---

3 **Flow control in a high-speed bus-based ATM switching hub**
Song Chong; Ramesh Nagarajan; Yung-Terng Wang;
Broadband Switching Systems, 1997. Proceedings. 2nd IEEE International Workshop on , 2-4 Dec. 1997
Pages:137 - 147

[Abstract] [PDF Full-Text (1012 KB)] **IEEE CNF**

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4 **The GIGAswitch control processor**
Walsh, R.J.; Ozveren, C.M.;
Network, IEEE , Volume: 9 , Issue: 1 , Jan.-Feb. 1995
Pages:36 - 43

[Abstract] [PDF Full-Text (712 KB)] **IEEE JNL**

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(high speed) and bus <and>control* and port and se [Search]

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **A parallel, high speed circular queue structure**
Barbour, A.E.; Alhayek, I.;
Circuits and Systems, 1989., Proceedings of the 32nd Midwest Symposium or
16 Aug. 1989
Pages:1089 - 1092 vol.2

[Abstract] [PDF Full-Text (320 KB)] **IEEE CNF**

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A low cost, high speed portable communications device: a case study using IDT RV4640 microprocessor & IDT77903 ATM card

Kakkar, S. Hussain, A.B.
Integrated Device Technol. Inc., Santa Clara, CA , USA;

This paper appears in: **Compcon '97. Proceedings, IEEE**

Meeting Date: 02/23/1997 - 02/26/1997
Publication Date: 23-26 Feb. 1997
Location: San Jose, CA USA
On page(s): 172
Reference Cited: 0
Number of Pages: xvi+342
Inspec Accession Number: 5552892

Abstract:
Summary form only given, as follows. We present a design for a low cost but powerful and **high speed** communications device powered by IDT's RV4640 as its processing engine. The device can achieve very **high speed**, thanks to the PCI **bus** compatible IDT ATM NIC. The device could be used as a two way pager, a set-top box, an Internet terminal, a personal digital assistant or as a video phone. The RV4640 is a very affordable 64 bit RISC processor that executes 175 dhrystone MIPS at 133 MHz. The

RV4640 can be connected to a System Interface Chip which will provide I/O and **memory control**. The IDT77903 ATM card is a full duplexed 25 Mbps NIC with a PCI **bus** interface and it costs less than $100 (US). Integrating this card into our device as a network interface will make highspeed videoconferencing and multimedia applications easily implementable

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Index Terms:

add-on boards   mobile communication   multimedia systems   network interfaces   **portable** computers   reduced instruction set computing   system buses   teleconferencing   videotelephony   64 bit RISC processor   IDT RV4640 microprocessor   IDT77903 ATM card   Internet terminal   PCI **bus** compatible IDT ATM NIC   PCI **bus** interface   System Interface Chip   case study   full duplexed 25 Mbps NIC   highspeed videoconferencing   low cost **high speed portable** communications device   **memory control**   multimedia applications   network interface   personal digital assistant   processing engine   set-top box   two way pager   video phone

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Flow control in a high-speed bus-based ATM switching hub

Song Chong Ramesh Nagarajan Yung-Terng Wang
Dept. of Electron. Eng., Sogang Univ., Seoul, South Korea;

This paper appears in: **Broadband Switching Systems, 1997. Proceedings. 2nd IEEE International Workshop on**

Meeting Date: 12/02/1997 - 12/04/1997
Publication Date: 2-4 Dec. 1997
Location: Taiwan China
On page(s): 137 - 147
Reference Cited: 5
Number of Pages: 187
Inspec Accession Number: 5998256

Abstract:
Studies flow **control** in a **high-speed bus**-based ATM switching hub for premises switching. The switching fabric is a dual-**bus** with slots for diverse **port** cards that interface to the external world. There can be a significant discrepancy in the switching fabric speed and the **port** card speed. This can result in buffer overflows at the receiving **port** buffer and consequently high losses in the switching fabric. Adequate flow **control** mechanisms are necessary. This paper first examines two different flow **control** strategies. Then we consider a third hybrid strategy which combines the strengths of the

first two strategies. In the first flow **control** scheme, physical flow **control**, all streams destined to a receiver with buffer problems such as high occupancy and loss are shut down till the congestion is cleared. This scheme has the advantage that loss is severely limited but has the disadvantage that high-rate streams arriving at this buffer can in some circumstances starve lower-rate streams. In a second strategy, logical flow **control**, streams are implicitly selected based on their rates and shut down. This scheme has the advantage that the higher-rate streams will eventually be shut down more often and hence cannot overwhelm the lower-rate streams. However, loss is not easily **controlled** in this scheme. Finally, in a hybrid strategy, we combine physical and logical flow **control** with logical **control** activated first and physical **control** activated later when the logical **control** is unable to limit the buffer occupancy and loss. This hybrid strategy is the recommended choice for flow **control** in the setting of interest

Index Terms:

asynchronous transfer mode buffer **storage** telecommunication congestion **control** buffer overflows congestion dual-**bus** flow **control** high-rate streams **high-speed bus**-based ATM switching hub hybrid strategy logical flow **control** losses low-rate streams occupancy physical flow **control** **port** card speed premises switching receiving **port** buffer switching fabric speed

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L3: Entry 6 of 7 File: USPT Jul 8, 1997

DOCUMENT-IDENTIFIER: US 5646651 A
TITLE: Block mode, multiple access multi-media/graphics memory

Abstract Text (1):
The integration of Video and Graphics Rasterization along with associated functional blocks provides a balanced MultiMedia/Graphics solution to the technology/bandwidth problem of today's higher density memories. Video rasterization, graphic rasterization, and window identifier functionality are contained on the same chip, fast Random Access Memory for each is provided for each, and the wide bus and high speed accesses to within the chip are shared and contained. The problem is therefore solved in a manner beneficial to both rasterization and video components of Multi-Media and Graphics. Window identification and control functions are added into the memory module, thus permitting both video and graphics rasterization functionality to be closely coupled to an independent high speed SRAM within the Memory Module, and thus applying the full internal wide bus bandwidth of the Frame Buffer memory to both real time video Multi-Media and graphics rasterization functions.

Detailed Description Text (4):
The Rasterizer 200 also contains a smaller FIFO as small as 64 bits to buffer graphic data while the Graphic SRAM 210 is not available. The Arbiter/Controller 290 synchronizes and schedules the accesses of the separate memory components (the video SRAM 250 and WIDs, the graphic SRAM 210 and WIDs, the Serial Access Memory 260, and the Frame buffer 220) for video, rasterization, and screen refresh operations.

Detailed Description Text (5):
This scheduler function is key to balancing the loads and making the most of the high bandwidth interface to memory within the MGRAM for the combined video/graphics functionality. Since video frames are generally sequential through memory, the writing of one video block and reading of the adjacent video block (and associated WIDs) may be accomplished within one memory access. If the Video I/F 240 needs to update a block that is currently being updated in the Graphic SRAM 210, it is the Arbiter/Controller 290 that causes the Rasterizer 200 functions to suspend while that block is sent through the multiplexer 230 to the Video SRAM 250 for video update. The modified block is then redirected back to the Graphic SRAM 210 and the Rasterizer function is restarted. The Arbitor/Controller 290 also controls routine Frame Buffer/WID memory 220 refresh cycles and data transfer to the SAM 260 port.

Detailed Description Text (9):
The SAM 260 is the Serial Access Memory that provides the serialization function between the Frame Buffer 220 and the Palette portion of the Palette/VMUX/WIX 270. The SAM 260 converts parallel data from the frame buffer 220 to a serial stream of 4 pixels width. The WIX portion of the Palette/VMUX/WIX 270 provides a programmable Window Identifier index function that allows the programming and lookup of the WID bit's meaning.

Detailed Description Text (22):
The integration of Video and Graphics Rasterization along with associated functional blocks as described herein, provides a balanced Multi-Media/Graphics

solution to the technology/bandwidth problem of today's higher density memories. By containing both video, graphic rasterization, and window identifier functionality on the same chip, by providing fast Random Access Memory for each, and by sharing and containing the wide bus and high speed accesses to within the chip, a unique and effective solution is thereby provided. The problem is therefore solved in a manner beneficial to both rasterization and video components of Multi-Media and Graphics.

Detailed Description Text (24):
In summary, the MGRAM provides for Video Interface through a Video Transfer Channel (VTC) to a high speed static memory, graphics interface through a processor bus and graphics rasterization primitives to a separate high speed static memory, and wide bus interface to the Frame buffer and Serial Access Memory (SAM) all of which are contained within the MGRAM module. The unique combination of video, rasterizer, Video SRAM, and Window Identifiers (WID) to identify the individual types of pixels, solves the technology/bandwidth problem in a manner allowing both video and graphics to share the high bandwidth Frame Buffer co-operatively.

CLAIMS:

1. A multi-media/graphics random access memory module integrated on a single chip comprising:

a video interface connected to input pins for receiving data from a video transfer channel;

a video static random access memory connected to said video interface to store data received from the video transfer channel;

a rasterizer connected to input pins for receiving data from a processor bus;

a graphic static random access memory connected to said rasterizer to store data received from the processor bus, said video and graphic static random access memories allowing for concurrent updating of both video and graphics;

a frame buffer for storing data to be displayed;

a palette providing a table lookup function for generating multi-bit color outputs;

a serial access memory to serialize data from the frame buffer to the palette;

a wide bus interface between the frame buffer and serial access memory and the video and graphic static random access memories; and

a multiplexer connected to the video and graphic static random access memories for providing a multiplexing function to match a data width of the video static random access memory to the serial access memory and a data width of the graphic static random access memory to the frame buffer allowing multi-media sharing of the internal bandwidth of the module.

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L3: Entry 6 of 7 File: USPT Jul 8, 1997

US-PAT-NO: 5646651
DOCUMENT-IDENTIFIER: US 5646651 A

TITLE: Block mode, multiple access multi-media/graphics memory

DATE-ISSUED: July 8, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Spannaus; John	Austin	TX	78733	
MacInnis; Alexander G.	San Carlos	CA	94070	

APPL-NO: 08/ 355875 [PALM]
DATE FILED: December 14, 1994

INT-CL: [06] G09 G 5/00

US-CL-ISSUED: 345/185; 345/201
US-CL-CURRENT: 345/519; 345/536, 345/546

FIELD-OF-SEARCH: 345/185, 345/113-120, 345/201, 345/198, 395/162-166, 395/148, 395/154, 395/157, 395/158, 395/340, 395/343, 395/501, 395/508, 395/806, 348/552, 348/564-567

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5392396	February 1995	MacInnis	395/164
☐	5402147	March 1995	Chen et al.	345/115
☐	5438663	August 1995	Matsumoto et al.	395/162

OTHER PUBLICATIONS

Bradley, et al., "User Interface for Adjusting Video Source Area", IBM Technical Disclosure Bulletin, V36 N09A, dtd Sep. 1993, pp. 449-452.
MacInnis, "Tear-Free Updates of Video and Graphics", IBM Technical Disclosure Bulletin, V36 N09A, dtd Sep. 1993, pp. 341-342.
MacInnis, "Clipping and Overlay of Multiple Sources of Video and Graphics in Display Windows", IBM Technical Disclosure Bulletin, V36 N09A, dtd Sep. 1993, pp. 105-106.

Chen, et al., "Input Locking for an Integrated (Single) Frame Buffer", IBM Technical Disclosure Bulletin, V36 N07, dtd Jul. 1993, pp. 539-540.
Pascoe, "Manual Multiple Source Selection in Computer-Assisted Video Conference", IBM Technical Disclosure Bulletin, V34 N7A, dtd Dec. 1991, pp. 380-381.
Bealkowski, et al. "Prioritizing Video Pixel Selection", IBM Technical Disclosure Bulletin, V32 N11, dtd Apr. 1990, pp. 195-198.

ART-UNIT: 245

PRIMARY-EXAMINER: Powell; Mark R.

ASSISTANT-EXAMINER: Loui; Martin

ATTY-AGENT-FIRM: Whitham, Curtis, Whitham & McGinn Emile; Volel

ABSTRACT:

The integration of Video and Graphics Rasterization along with associated functional blocks provides a balanced MultiMedia/Graphics solution to the technology/bandwidth problem of today's higher density memories. Video rasterization, graphic rasterization, and window identifier functionality are contained on the same chip, fast Random Access Memory for each is provided for each, and the wide bus and high speed accesses to within the chip are shared and contained. The problem is therefore solved in a manner beneficial to both rasterization and video components of Multi-Media and Graphics. Window identification and control functions are added into the memory module, thus permitting both video and graphics rasterization functionality to be closely coupled to an independent high speed SRAM within the Memory Module, and thus applying the full internal wide bus bandwidth of the Frame Buffer memory to both real time video Multi-Media and graphics rasterization functions.

5 Claims, 2 Drawing figures

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L3: Entry 7 of 7 File: USPT May 14, 1996

DOCUMENT-IDENTIFIER: US 5517626 A
TITLE: Open high speed bus for microcomputer system

Brief Summary Text (9):
Provided is an "Advanced Chip Interconnect" (ACI) bus, which is an open, high-speed local system bus. Decoupled from the I/O, ACI provides a consistent interface to the CPU subsystem, memory subsystem, graphics subsystem and peripheral subsystem.

Detailed Description Text (111):
CPU.sub.-- RESET is a processor only reset initiated under software control. The sources for CPU.sub.-- RESET are the keyboard controller and in the case of MCA System Control Port A. CPU.sub.-- RESET is also asserted on detection of the 386/486 special cycle shutdown. The cache controller will provide a method to mask the bus CPU.sub.-- Reset and also provide a register for a private version of CPU reset.

Detailed Description Text (332):
This Control Register contains the content of ports 22h and 23h, the device.sub.--id that the processor master is interrogating. When the processor accesses port 27h for read or write, the device which compares the DR successfully with DIDR will process the data. In case the index register points to any phantom CSRs, the selected chip, will be required to respond with SRDY# and send garbage data with proper parity to the processor. The processor can test CSR existence by first writing followed by reading the CSR location. If the contents don't match, then the CSR does not exist.

Detailed Description Text (344):
Bit 0 This Control Register indicates if I/O programming via ports 22h, 23h, 26h and 27h is enabled. This feature is added to allow these ports to be ignored for compatibility if there exists an I/O conflict. This bit defaults to 0. Once this bit is set all accesses to ports 23h, 24h, 26h and 27h are ignored. The only way to restore access to ports is to reset the chips.

Detailed Description Text (350):
Bit 1 Alternate A20 Gate. This bit is logically ORed with the keyboard controller A20 gate and in the case of an MCA machine also logically ORed with system control port A. Setting this bit to 1 enables address A20 to operate normally. When this bit, keyboard controller and system control port A's A20 are all 0, A20 is disabled from the processor and set to 0. This bit defaults to 0.

Detailed Description Text (390):
For ISA machines the configuration information is stored in an extended CMOS RAM. This RAM is similar to the MCA CMOS RAM, using the same addressing technique, ports 74h-76h. Access to the extended CMOS RAM is controlled through a CSR bit, which can enable/disable the CMOS RAM. This is to provide protection for the CMOS RAM area and ISA compatibility for normal port 70h-71h aliasing. As an lower cost alternative to the CMOS RAM almost any other non-volatile memory device can be used. One example is a serial non-volatile memory device requiring a clock and

single bit data. The clock is generated by using the port 74h decode, and data read and write can be one bit of the data port 76h.

Detailed Description Text (572):
These two Control Registers contain the content of port 22h and 25h, the device.sub.-- id that the processor master is interrogating. When the processor accesses port 27h for read or write, the device which compares the DR successfully with DIDR will respond with.SRDY# and process the data. In case the index register points to any phantom CSRs, the selected chip, the memory controller in this case, will be required to respond with SRDY# and send garbage data with proper parity to the processor. The processor can test CSR existence by first writing followed by reading the CSR location. If the contents don't match, then the CSR does not exist.

Detailed Description Text (636):
2.6.3.4.4 SCPB, System Control Port B (index 53h, port 61h)

Detailed Description Text (637):
This Control Register mimics the port 61h contents for compatibility. It is a passive port in the Memory Controller. The same port (master) appears in PIC, the Peripheral Interface Controller.

Detailed Description Text (1354):
The 86C150 Peripheral Interface Controller (PIC) provides support for the standard I/O devices in PC/AT and PS/2 compatible systems. The 86C150 integrates two "8259A" equivalent programmable interrupt controllers, one 8254 compatible timer, a watchdog timer, a parallel port, two serial ports, two system control registers, a card setup port and variety of system status/control ports and functions. Address decodes are also provided for floppy disk controller, keyboard controller, the real-time clock and 2K configuration RAM.

Detailed Description Text (1360):
The PIC integrates two "8259A" equivalent programmable interrupt controllers which support 15 level of interrupts and three timers for system (timer 0), audio tone generation (timer 2) and watchdog function (timer 3, for PS/2 only). The parallel port is compatible with PC/AT and additionally it also supports Micro Channel Architecture compatible "extended mode" which is bi-directional data transfers. Two "16550-equiv" serial port controllers are also integrated. The PIC also integrates the card setup port (96H) which select one of 8 adapter cards within the system, and system control port A(92H) port B(61H) for the control/status information of the system. Address decodes are provided for variety of system board resident I/O devices including floppy disk controller, keyboard controller, the real-time clock and 2K SRAM.

Detailed Description Text (1415):
GATE2 is controlled by bit 0 of port hex 061. Setting this bit causes GATE2 to go high.

Detailed Description Text (1427):
The system treats the programmable interval timer as an arrangement of five external I/O ports. Three ports are treated as count registers and two are control registers for mode programming. Counters are programmed by writing a control word and then an initial count. The count must follow the count format specified in the control word.

Detailed Description Text (1430):
Before accessing port 0040h, port 0043 must be programmed with the appropriate control word followed by an initial count value to port 0040h.

Detailed Description Text (1432):

Before accessing port 0042h, port 0043h must be programmed with the appropriate control word, followed by an initial count value to port 0042h.

Detailed Description Text (1433):
Port Hex 0043--Control Byte--Channel 0 or 2

Detailed Description Text (1435):
Before accessing port 0044h, port 0047 must be programmed with the appropriate control word, following by an initial count value to port 0044h.

Detailed Description Text (1446):
In the extended mode, a write operation to this port latches the data but it is only presented to the connector pins if the direction bit was set to Write in the parallel control port. A read operation in the extended mode produces either:

Detailed Description Text (1447):
1) The data previously written if the direction bit in the parallel control port is set to Write.

Detailed Description Text (1451):
2.4.6 PARALLEL PORT CONTROL PORT

Detailed Description Text (1452):
The parallel control port is a read or write port. A write operation to this port latches the six least-significant data bits of the bus. The sixth bit corresponds to the direction control bit and is only applicable in the extended mode. The remaining five bits are compatible with previous implementations as shown in the following figure. A read operation to the parallel control port presents the system microprocessor the data that was last written to it, with the exception of the write-only direction bit.

Detailed Description Text (1453):
2.5 SYSTEM CONTROL PORT A AND PORT B

Detailed Description Text (1455):
2.5.1 SYSTEM CONTROL REGISTER A; PORT 0092H

Detailed Description Text (1457):
2.5.2 SYSTEM CONTROL REGISTER B; PORT 0061H

Detailed Description Text (1460):
The integrated I/O functions of the system board use POS information during the setup procedure. The diskette drive controller, serial port, and parallel port are treated as a single device. Although the VGA is an integrated part of the system board, POS treats it as a separate device. The Setup Enable register is used to place the system board or the video subsystem into setup.

Detailed Description Text (1463):
2.6.2 SYSTEM BOARD I/O PORT CONTROL (POS 0102H)

Detailed Description Text (1464):
When bit 7 of the Setup Enable Register is set to 0, the diskette drive controller, serial and parallel interfaces are controlled by a bit pattern written to port 0102H, the System Board I/O byte.

Detailed Description Text (1471):
2.7.2 MEMORY CONTROL REGISTER (PORT 0103H)

Detailed Description Text (1472):
The port at address 0103H controls the refresh rate to the memory and enables the

system board RAM memory. To access this register, I/O address 0096H bit 3 must be set to 0 to avoid sending a `setup` signal to one of the channel connectors. Also, I/O address 0094H bit 7 must be set to 0, causing the system board to accept setup cycles. After accessing the Memory Control Register, I/O address 0094H, bit 7 must be set to 1. The register is accessed using I/O address 0103H and is Write-Only.

Detailed Description Text (1475):
The serial port controller provides the following functions:

Detailed Description Text (1496):
The PIC integrates two serial ports into the chip. It is configured and enabled by ESR: 1 (extended setup register 1). In IBM mode, only one serial port is selected. The selection of either port is determined by the bit 7 of the system board setup enable register (Hex 0094) and bit 3 of the system board I/O byte (Hex 0102). When bit 7 of the setup enable register is set to 0, the serial port is controlled by bit 3 of the system board I/O byte. A 1 in bit 3 sets the serial port as serial 1, and a 0 sets it as serial 2. When configured as serial 1, the I/O address is at 03F8-03FF Hex. As serial 2, the port is at address 02F8-02FF Hex.

Detailed Description Paragraph Table (9):
bit 7:4 IBM reserved, defaults 1110 bit 3 ENSPLIT, split, default 0 0 split enabled, relocations mapped by Split Address Register 1 split disabled bit 2 SIZ640, base memory, default 0 0 split at 640 K, (type 3 & 4 machines only support split at 640K) 1 split at 512 K bit 1 ROMEN, BIOS shadow, defaults 1 0 E & F segment in DRAM read from DRAM, write to channel 1 E & F segment in ROM read from ROM, write to RAM bit 0 ENPRPCH, parity enable, defaults 1 0 memory parity enable 1 memory parity disabled, (for compatibility with other systems, enabling and disabling of parity checking should be done through system control port B at port 61h)

Detailed Description Paragraph Table (80):
Port Hex 0047 - Control Byte - Channel 3
This is write only register. The bit definitions are as follow: Counter Control Bit Assignments Port 47 Hex Bits Label Function
7, 6 SC1, SC0 Counter Select 0 0 Select Counter 3 0 1 Reserved 1 0 Reserved 1 1 Reserved
5, 4 RW1, RW0 Byte Select
0 0 Counter Latch Command 0 1 Read/Write Counter Bits 0-7 only 1 0 Reserved 1 1 Reserved 3, 2, 1, 0 Must be = 0 Mode 0 and Binary count only

Detailed Description Paragraph Table (95):
Address Device
0000-001F DMA Controller 0020, 0021 Interrupt Controller 1, 8259AA 0040, 0042, 0043, 0044, 0047 System Timers 0060 Keyboard Auxiliary Device 0061 System Control Port B 0064 Keyboard Auxiliary Device 0070, 0071 RT/CMOS and NMI Mask 0074, 0075, 0076 Reserved 0081, 0082, 0083, 0087 DMA Page Register (0-3) 0089, 008A, 008B, 008F DMA Page Register (4-7) 0090 Central Arb. Control Port 0091 Car Select Feedback 0092 System Control Port A 0093 Reserved 0094 System Board Setup 0096, 0097 POS, Channel Connector Select 00A0, 00A1 Interrupt Controller 2, 8259AA 00F0-00FF Math Coprocessor 0100-0107 Programmable Option Select 0278-027B Parallel Port 3 02F8-02FF serial port 2 (RS-232-C) 0378-037B Parallel Port 2 03BC-03BF Parallel Port 1 03B4, 03B5, 03BA, 03C0-03C5 Video Subsystem 03CE, 03CF, 03D4, 03D5, 03DA Video Subsystem 03C6-03C9 Video DAC 03F0-03F7 Diskette Drive Controller 03F8-03FF Serial Port 1 (RS-232-C)

Detailed Description Paragraph Table (97):
Address Description
Programmable Interrupt Controller 0020 ICW1,

OCW2, OCW3 (Write) PIC#1 0020 IRR, ISR/Interrupt level (Read) PIC#1 0021 ICW2, ICW3, ICW4, OCW1 (Write) PIC#1 0021 IMR (Read) PIC #1 00A0 ICW1, OCW2, OCW3 (Write) PIC#2 00A0 IRR, ISR/Interrupt level (Read) PIC#2 00A1 ICW2, ICW3, ICW4, OCW1 (Write) PIC#2 00A1 IMR (Read) PIC #2 Programmable Timer/Counter 0040 Counter#0 (Read/Write) 0042 Counter#2 (Read/Write) 0043 Control word for counters #0 & #2 (write) 0044 Counter#3 (Read/Write) 0047 Control word for counters #3 (write) Keybord/Auxiliary Device Controller 0060 8042 Keyboard Controller data port (Read/Write) 0064 8042 Keyboard Controller command/status port (R/W) Real Time Clock (RTC), CMOS RAM Control 0070 RTC/CMOS and NMI Mack (Write) 0071 RTC/CMOS data port (Read/Write) 0074 extended CMOS Ram Address (Write) 0075 extended CMOS Ram Address (Write) 0076 extended CMOS Ram data port (Read/Write) System Control Port 0061 System Control Port B 0092 System Control Port A Micro Channel Control 0090 Central Arbitration register (Read/Write) 0091 Card Selected Feedback 0094 System Board Enable/setup register 0095 Reserved 0096 Adapter Enable/Setup register 0097 Reserved 0100 POS register 0 - System/Adapter ID Byte (LSB) 0101 POS register 1 - System/Adapter ID Byte (MSB) 0102 POS register 2 - Option Select Data Byte 0103 POS register 3 - Option Select Data Byte 2 0104 POS register 4 - Option Select Data Byte 3 0105 POS register 5 - Option Select Data Byte 4 0106 POS register 6 - Sub-address Extension (LSB) 0107 POS register 7 - Sub-address Extension (MSB) Serial I/O Port Bit 7 of Line Control Reg. F8 Transmitter Holding register (W) 0 03F8 Receiver Buffer register (R) 0 03F8 divisor Latch, Low Byte (R/W) 1 03F9 divisor Latch, High Byte (R/W) 1 03F9 Interrupt Enable Register (R/W) 0 03FA Interrupt Identification Register (R)X 03FA FIFO CONTROL register (W) X 03FB Line Control register (R/W) X 03FC Modem Control Register (R/W) X 03FD Line Status register (R) X 03FE Modem Status register (R) X 03FF Scratch Register (R/W) X Secondary Serial Port Bit 7 of Line Control Reg. 02F8 Transmitter Holding register (W) 0 02F8 Receiver Buffer register (R) 0 02F8 divisor Latch, Low Byte (R/W) 1 02F9 divisor Latch, High Byte (R/W) 1 02F9 Interrupt Enable Register (R/W) 0 02FA Interrupt Identification Register (R)X 02FA FIFO CONTROL register (W) X 02FB Line Control register (R/W) X 02FC Modem Control Register(R/W) X 02FD Line Status register (R) X 02FE Modem Status register (R) X 02FF Scratch Register (R/W) X Parallel Port 1: 03BC Data Port (R/W) 03BD Status Port (R) 03BE Control Port (R/W) 03BF Reserved Parallel Port 2: 0378 Data Port (R/W) 0379 Status Port (R) 037A Control Port (R/W) 037B Reserved Parallel Port 3: 0278 Data Port (R/W) 0279 Status Port (R) 027A Control Port (R/W) 027B Reserved Math Coprocessor 00F0 Coprocessor Clear Busy 00F1 Coprocessor Reset VGA Subsystem 03BA Input Status Register 1 (R) Monoch rome Emulation 03BA Feature Control Register (W) Monochrome Emulation 03DA Input Status Register 1 (R) Color Emulation 03DA Feature Control Register (W) Color Emulation 03C2 Miscellaneous Output Register (W) 03C2 Input Status Register (R) 03CC Miscellaneous Output Register (R) 03CA Feature Control Register (R) 03C3 Video Subsystem Enable (R/W) Attribute registers: 03B4 Index register (R/W) Monochrome Emulation 03B5 other CRT Controller register (R/W) Monochrome Emulation D4 Index register (R/W) Color Emulation 03D5 other CRT Controller register (R/W) Color Emulation Sequencer Register 03C4 Address Register (R/W) 03C5 Other Sequencer Registers (R/W) Graphics Registers 03CE Address Register 03CF Other Graphics Registers DAC Registers 03C6 FEL Mask (R/W) 03C7 DAC State Register (R) 03C7 PEL Address (Read Mode) (R/W) 03C8 PEL Address (Write Mode) (R/W) 03C9 PEL Data Register (R/W) Diskette Drive Controller 03F0 Status Register A (R) 03F1 Status Register B (R) 03F2 Digital Output Register (W) 03F3 Reserved 03F4 Diskette Drive Controller Status Register (R) 03F5 Data Register (R/W) 03F6 Reserved 03F7 Digital Input Register (R) Interrupt Assignments Level Function NMI Parity Watchdog Timer Arbitration time-out channel check IRQ0 Timer IRQ1 Keyboard IRQ2 Cascaded IRQ8 Real Time Clock IRQ9 Redirect Cascade IRQ10 Reserved IRQ11 Reserved IRQ12 Mouse IRQ13 Math Coprocessor Exception IRQ14 Fixed Disk IRQ15 Reserved IRQ3 Secondary Serial Port IRQ4 Primary Serial Port IRQ5 Reserved IRQ6 Diskette IRQ7 Parallel Port

First Hit Fwd Refs

End of Result Set

Generate Collection Print

L3: Entry 7 of 7 File: USPT May 14, 1996

US-PAT-NO: 5517626
DOCUMENT-IDENTIFIER: US 5517626 A

TITLE: Open high speed bus for microcomputer system

DATE-ISSUED: May 14, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Archer; Jordan J.	San Jose	CA		
Deora; Ajit J.	San Jose	CA		
Leung; Kent S.	Milpitas	CA		
Peng; Leon	Mountain View	CA		
Schopmeyer; Robert C.	Los Altos	CA		
Scott; David J.	Gilroy	CA		
Sharma; Sanjay	Sunnyvale	CA		
Stevens; Virgil	Rounonent	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
S3, Incorporated	Santa Clara	CA			02

APPL-NO: 08/ 011449 [PALM]
DATE FILED: January 29, 1993

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATIONS This application is a divisional application of U.S. patent application Ser. No. 07/521,042, filed May 7, 1990, entitled "Microcomputer System with Open High Speed Bus", now abandoned.

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/290; 395/306, 395/445, 395/285
US-CL-CURRENT: 710/110; 710/105, 711/118

FIELD-OF-SEARCH: 395/325, 395/725, 395/425, 395/275, 395/290, 395/306, 395/457, 395/445, 395/853, 395/733, 395/735

PRIOR-ART-DISCLOSED:

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Search Selected Search ALL Clear

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☐	4543628	September 1985	Pomfret	395/275
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☐	5274780	December 1993	Nakao	395/325

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Digital Bus Handbook, Joseph DiGiacomo, ed., Chapters 5-7, McGraw-Hill Publishing Company, 1990.

ART-UNIT: 235

PRIMARY-EXAMINER: Auve; Glenn A.

ATTY-AGENT-FIRM: Skjerven, Morrill, MacPherson, Franklin & Friel Klivans; Norman R.

ABSTRACT:

An open high-speed local system bus for a microcomputer system which is decoupled from I/O and provides a consistent interface to the CPU subsystem, memory subsystem, graphics subsystem and peripheral subsystem. The local system bus supports discrete and burst transactions, pipelining in both the transactions, multiple microprocessor and distributed interrupts.

44 Claims, 95 Drawing figures

US-PAT-NO: 6320711

DOCUMENT-IDENTIFIER: US 6320711 B1

TITLE: High-speed unified data interface for a read channel in a disk drive system

---------- KWIC ---------

Brief Summary Text - BSTX (4):

A magnetic disk system stores user data in data tracks on the surface of a disk device. The user data is transferred between the disk and the user as follows. A head is positioned over a circular data track and reads the user data as the disk spins. The head transfers the user data to a pre-amp, and the pre-amp transfers the user data to a read channel integrated circuit. The read channel integrated circuit processes and transfers the user data to a drive manager integrated circuit over a high-speed bus, such as a Non-Return to Zero (NRZ) bus. The drive manager integrated circuit transfers the user data to the user.

Detailed Description Text - DETX (6):

The read channel integrated circuit 103 uses a multiplexer to exchange user data and other data with the disk control integrated circuit 104 over a data bus, such as a high-speed Non-Return to Zero (NRZ) bus. The read channel integrated circuit 103 exchanges the user data with the data bus when the disk device 102 is reading the user data and is not reading the servo data. The read channel integrated circuit 103 exchanges the other data with the data bus when the disk device 102 is reading the servo data and is not reading the user data. Some examples of the other data include servo data, read channel settings, and read channel performance data. The read channel integrated circuit 103 could be adapted from the model # ADRT 1000 supplied by Analog Devices.

Detailed Description Text - DETX (13):

FIG. 3 depicts a disk drive system 301 that is known in the art. The disk device 102 contains the user data 211 and the server data 212. The read channel integrated circuit 303 comprises signal processor 320, configuration registers

US006320711B2

(12) United States Patent
Hill

(10) Patent No.: US 6,320,711 B2
(45) Date of Patent: *Nov. 20, 2001

(54) HIGH-SPEED UNIFIED DATA INTERFACE FOR A READ CHANNEL IN A DISK DRIVE SYSTEM

(75) Inventor: John F. Hill, Nederland, CO (US)

(73) Assignee: STMicroelectronics N.V. (NL)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/072,276

(22) Filed: May 4, 1998

Related U.S. Application Data

(60) Provisional application No. 60/066,701, filed on Nov. 25, 1997.

(51) Int. Cl.[7] G11B 5/09; G11B 5/596

(52) U.S. Cl. 360/46; 360/41; 360/77.08

(58) Field of Search 360/41, 46, 65, 360/75, 77.08

(56) References Cited

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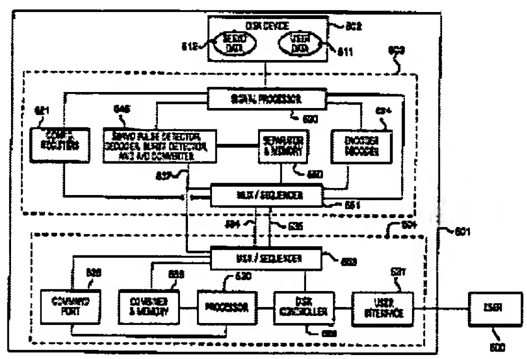
* cited by examiner

Primary Examiner—David Hudspeth
Assistant Examiner—Regina Y. Neal
(74) Attorney, Agent, or Firm—Lisa K. Jorgenson; William J. Kubida

(57) ABSTRACT

The invention provides a high-speed interface that transfers user data and other data over a single unified interface between a read channel integrated circuit and another integrated circuit, such as the drive control integrated circuit. The high-speed interface eliminates the need for analog pins on the integrated circuits to lower the cost of the system. The high-speed interface also eliminates the use of the serial interface to transfer the servo position data and other data which speeds up the data transfer. Examples of the other data include read channel settings, read channel performance data, and servo data. A read channel integrated circuit exchanges the user data with a data bus when the disk drive system is reading or writing the user data. The read channel integrated circuit exchanges the other data with the data bus when the disk drive system is reading servo data. The other integrated circuit exchanges the user data with the data bus when the disk drive system is reading or writing the user data. The other integrated circuit exchanges the other data with the data bus when the disk drive system is reading the servo data. The data bus transfers the user data and the other data between the integrated circuits.

22 Claims, 4 Drawing Sheets



US-PAT-NO: 5970069

DOCUMENT-IDENTIFIER: US 5970069 A

TITLE: Single chip remote access processor

---------- KWIC ---------

Drawing Description Text - DRTX (47):
FIGS. 89a-90a are diagrams illustrating PCI port control registers.

Detailed Description Text - DETX (21):
In addition, when the first packet is sent through a particular communication interface, CPU 90 performs a call sequence to setup the desired connection through the corresponding controller. For example, CPU 90 provides SWAN controllers 76a-76d with a telephone number and other data to initiate a call over interface ports 40, 42a and 42b.

Detailed Description Text - DETX (28):
When serial data is received at V.34 Codec interface 44, the data represents a sampling of the analog signal transmitted over a public switched telephone network. The sampling is performed by an external V.34 Codec (not shown) coupled to V.34 Codec interface 44. As in the case where serial data is received at one of the LAN or WAN ports DMA controller 82 collects the serial data and stores the data in local memory, through memory controller 110. Once the data samples have been stored in local memory, CPU 90 retrieves the data samples and demodulates the samples into digital data packets by performing a digital filter and data pump function through the V.34 digital signal processing algorithm. CPU 90 then stores the data packets back into local memory through memory controller 110, and notifies the routing software executed by CPU 90 to look for the packets in local memory. The routing software then retrieves the packets from local memory and determines their destination, as discussed above.

Detailed Description Text - DETX (65):
PCI.sub.-- INTn (PCI Interrupt): RAP asserts PCI.sub.-- INTn when the

US005970069A

United States Patent [19]

Kumar et al.

[11] **Patent Number:** 5,970,069

[45] **Date of Patent:** Oct. 19, 1999

[54] **SINGLE CHIP REMOTE ACCESS PROCESSOR**

[75] Inventors: Shailendra Kumar, San Jose, Calif.; Christopher D. Sonnek, North St. Paul, Minn.

[73] Assignee: LSI Logic Corporation, Milpitas, Calif.

[21] Appl. No.: 08/840,975

[22] Filed: Apr. 21, 1997

[51] Int. Cl.[6] H04L 12/28; H04J 3/16

[52] U.S. Cl. 370/402; 370/401; 370/466

[58] Field of Search 370/351, 355, 370/357, 360, 389, 401, 402, 465, 466, 463, 467

[56] References Cited

U.S. PATENT DOCUMENTS

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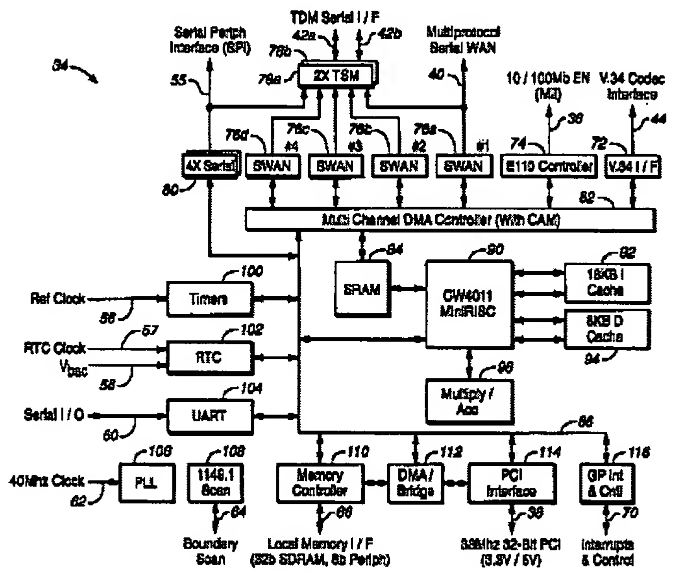
5,640,399 6/1997 Rostoker 370/402

Primary Examiner—Ajit Patel
Assistant Examiner—Ricardo M. Pizarro
Attorney, Agent, or Firm—Westman, Champlin & Kelly, P.A.

[57] **ABSTRACT**

A single chip integrated remote access processor circuit has a plurality of communication interface units, including a local area network (LAN) interface unit, a first multiprotocol serial wide area network (SWAN) interface unit, a telephony coder-decoder interface unit and a peripheral component interface (PCI) unit. A data routing control circuit is coupled to the plurality of communication interface units for controlling data transfer between the interface units.

18 Claims, 83 Drawing Sheets



US-PAT-NO: 5517626

DOCUMENT-IDENTIFIER: US 5517626 A

TITLE: Open high speed bus for microcomputer system

---------- KWIC ---------

Brief Summary Text - BSTX (9):
Provided is an "Advanced Chip Interconnect" (ACI) bus, which is an open, high-speed local system bus. Decoupled from the I/O, ACI provides a consistent interface to the CPU subsystem, memory subsystem, graphics subsystem and peripheral subsystem.

Detailed Description Text - DETX (111):
CPU.sub.-- RESET is a processor only reset initiated under software control. The sources for CPU.sub.-- RESET are the keyboard controller and in the case of MCA System Control Port A. CPU.sub.-- RESET is also asserted on detection of the 386/486 special cycle shutdown. The cache controller will provide a method to mask the bus CPU.sub.-- Reset and also provide a register for a private version of CPU reset.

Detailed Description Text - DETX (332):
This Control Register contains the content of ports 22h and 23h, the device.sub.-- id that the processor master is interrogating. When the processor accesses port 27h for read or write, the device which compares the DR successfully with DIDR will process the data. In case the index register points to any phantom CSRs, the selected chip, will be required to respond with SRDY# and send garbage data with proper parity to the processor. The processor can test CSR existence by first writing followed by reading the CSR location. If the contents don't match, then the CSR does not exist.

Detailed Description Text - DETX (344):
Bit 0 This Control Register indicates if I/O programming via ports 22h, 23h, 26h and 27h is enabled. This feature is added to allow these ports to be ignored for compatibility if there exists an I/O conflict. This bit defaults

US005517626A

United States Patent [19]

Archer et al.

[11] **Patent Number:** 5,517,626

[45] **Date of Patent:** May 14, 1996

[54] OPEN HIGH SPEED BUS FOR MICROCOMPUTER SYSTEM

[75] Inventors: Jordan J. Archer; Ajit J. Dacra, both of San Jose; Kent S. Leung, Milpitas; Leon Peng, Mountain View; Robert C. Schopmeyer, Los Altos; David J. Scott, Gilroy; Sanjay Sharma, Sunnyvale; Virgil Stevens, Roundtop, all of Calif.

[73] Assignee: S3, Incorporated, Santa Clara, Calif.

[21] Appl. No.: 11,449

[22] Filed: Jan. 29, 1993

Related U.S. Application Data

[62] Division of Ser. No. 521,042, May 7, 1990, abandoned.

[51] Int. Cl.[6] G06F 13/00

[52] U.S. Cl. 395/290; 395/306; 395/445; 395/285

[58] Field of Search 395/325, 725, 395/425, 275, 290, 306, 457, 445, 853, 753, 735

[56] References Cited

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Digital Bus Handbook, Joseph DiGiacomo, ed., Chapters 5–7, McGraw-Hill Publishing Company, 1990.

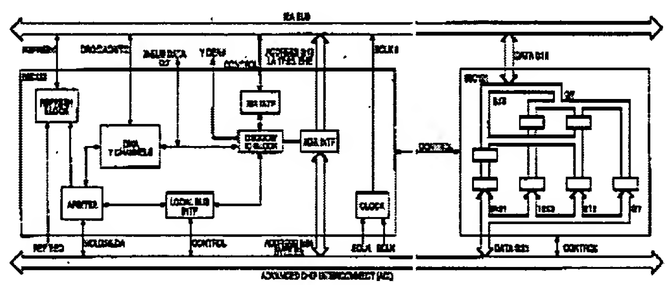
Primary Examiner—Glenn A. Auve

Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel; Norman R. Klivans

[57] ABSTRACT

An open high-speed local system bus for a microcomputer system which is decoupled from I/O and provides a consistent interface to the CPU subsystem, memory subsystem, graphics subsystem and peripheral subsystem. The local system bus supports discrete and burst transactions, pipelining in both the transactions, multiple microprocessor and distributed interrupts.

44 Claims, 92 Drawing Sheets



First Hit Fwd Refs
End of Result Set

Generate Collection Print

L4: Entry 1 of 1 File: USPT Dec 16, 2003

DOCUMENT-IDENTIFIER: US 6665807 B1
TITLE: Information processing apparatus

Detailed Description Text (10):
In FIG. 19, numeral 1901 denotes a processor, 1902 a main memory, and 1903 a ROM. Numeral 1904 denotes a companion chip which is a bus adapter formed by integrating peripheral functions together. Numeral 1905 denotes an I/O device (1) having a network interface function. The I/O device (1) 1905 is a separate device having an interface such as an extension substrate or a connector. Numeral 1906 denotes an I/O device (2) having a radio communication interface function. Numeral 1907 denotes an I/O device (3) having a stored media interface. Numerals 1908 and 1909 denote connectors. Numeral 1910 denotes a radio communication antenna, 1911 a stored media device, 1912 a processor bus, 1913 an I/O bus of the present invention, and 1914 a network such as a LAN. Numeral 1915 denotes an example of the range of components mounted on a mother board (printed-circuit board) of the present information processor. In FIG. 20, numeral 2001 denotes a CPU module, 2002 a CPU core, 2003 a cache memory, 2004 a cache memory controller, 2005 a TLB (translation look aside buffer) for address translation, 2006 a MMU (memory management unit), 2007 an interrupt controller, 2008 a bus controller of an internal peripheral bus, 2009 a real time clock module, 2010 a timer unit module, 2011 a serial communication interface module, 2012 an infrared ray interface module, 2013 an AD (analog/digital) converter module, 2014 a DA (digital/analog) converter module, 2015 a clock pulse generator/watch dog timer module, 2016 a DMA control module, 2017 an external bus interface, 2018 an internal high speed bus, 2019 an internal peripheral bus. In FIG. 21, numeral 2101 denotes a processor bus interface unit, 2102 a serial communication interface module, 2103 an AD/DA converter module, 2104 a liquid crystal controller module, 2105 a PC card interface module, 2106 a USB (universal serial bus) interface module, 2107 a bus protocol converter, and 2108 an I/O bus interface unit. In FIG. 22, numeral 2201 denotes an I/O device connected to an I/O bus of the present invention. Numeral 2202 denotes a clock generator for distributing a clock to modules connected to the processor bus. Numerals 2203 and 2204 denote a module (1) and a module (2) connected to a bus 2211, respectively. Numeral 2005 denotes a clock generator for distributing a clock to modules connected to the bus 2211. Numeral 2206 denotes a clock line for supplying the clock from the clock generator 2202 to the processor 1901. Numeral 2207 denotes a clock line for supplying the clock from the clock generator 2202 to the companion chip 1904. Numerals 2208 and 2209 denote clock lines for supplying the clock from the clock generator 2205 to the module (1) and module (2), respectively. Numeral 2210 denotes a clock line for supplying the clock from the clock generator 2205 to the I/O device 2201. Numeral 2211 denotes a bus for connecting modules beyond the I/O device 2201. Numeral 2212 denotes a data line of a bus of the present invention. Numeral 2213 denotes a source clock line of the bus of the present invention. (In the present embodiment, up and down source clock lines are separated into different clock lines. The source clock line 2213 is an input to the companion chip 1904.) Numeral 2214 denotes a source clock line of the bus of the present invention. (In the present embodiment, up and down source clock lines are separated into the different clock lines. The source clock line 2214 is an output from the companion chip 1904.) Numeral 2215 denotes a bus mastership

request signal sent from the I/O device 2201. Numeral 2216 denotes a bus use grant signal sent from a bus arbiter to the I/O device 2201. Numeral 2217 denotes a processor bus interface, and numeral 2218 denotes a transfer information buffer. Numeral 2219 denotes a synchronization circuit for synchronizing signals of different frequencies. Numeral 2220 denotes a bus arbiter for arbitrating a bus mastership of the I/O bus of the present invention. Numerals 2221 and 2222 denote transfer information buffers. Numeral 2223 denotes a transfer (transmission) controller. Numerals 2224, 2225, 2226 and 2227 denote flip-flops. Numeral 2228 denotes a source clock input buffer, 2229 an input buffer, 2230 an output buffer, 2231 a source clock output buffer, 2232 a clock buffer, and 2233 clock distribution wiring. Numeral 2234 denotes a range which operates according to a clock CK2 of the I/O device 2201. Numeral 2235 denotes a range which operates according to a clock CK1 of the processor bus. Numeral 2236 denotes a transfer (transmission) controller. Numeral 2237 denotes an interface of the bus 2211. Numerals 2238 and 2239 denote transfer information buffers. Numeral 2240 denotes a synchronization circuit for synchronizing signals of different frequencies. Numeral 2241 denotes a transfer information buffer. Numerals 2242, 2243, 2244 and 2245 denote flip-flops. Numeral 2246 denotes an output buffer, 2247 an input buffer, 2248 a source clock input buffer, 2249 a clock buffer, and 2250 clock distribution wiring. Numeral 2251 denotes a range which operates according to the clock CK1 of the companion chip 1904. Numeral 2252 denotes a range which operates according to the clock CK2 of the bus 2211 and the I/O device 2201. Numeral 2253 denotes a source clock output buffer, 2260 an output buffer, 2261 an input buffer, 2262 an input buffer, and 2263 an output buffer. Since FIG. 22 is a diagram showing data flow, and details of wiring of signal lines with respect to the processor bus I/F and the bus I/F having the function of the control system have no direct relation to the present invention, the details of wiring are omitted. Furthermore, numerals 2217, 2218, 2224, 2226 and 2222 in FIG. 22 correspond to the processor bus interface unit 2101 shown in FIG. 21. Numerals 2220, 2221, 2223, 2225, 2227, 2228, 2229, 2230 and 2231 in FIG. 22 correspond to the I/O bus interface unit 2108 in FIG. 21. The synchronization circuit 2219 in FIG. 22 is included in the protocol converter 2107 shown in FIG. 21. The peripheral devices such as the SCI 2102 and the LCDC 2104 shown in FIG. 21 are omitted in FIG. 22. The processor bus interface unit 2101 and the I/O bus interface unit 2108 may serve as an input circuit or an output circuit according to the sense of transfer. The clock is distributed from the clock distribution wiring 2233 to the circuit, such as the transfer controller 2223 and the buffer 2222, which operates according to CK1. In FIG. 23, numeral 2301 denotes a processor incorporating an adapter function for conducting protocol conversion to the I/O bus of the present invention. In FIG. 24, numeral 2401 denotes an external I/O bus interface, 2402 a liquid crystal controller module, 2403 a PC card interface module. In FIG. 25, numerals 2501 and 2502 denote receiving circuits, and numerals 2503 and 2504 denote circuits having a transmission function. In the companion chip 1904 shown in FIG. 22, a portion including the devices operating according to CK1, such as the processor bus I/F and the transmission controller, surrounded by a broken line is a circuit having the transmission function. A portion including the devices operating according to CK2, such as the buffer 2221, surrounded by a broken line is a receiving circuit. The SCI 2102, the ADC/DAC 2103, and the like shown in FIG. 21 are included in the circuit 2503 having the transmission function. By the way, in FIG. 22, the synchronization circuit is operating in synchronism with CK1, and consequently the synchronization circuit is included in the circuit having the transmission function.

First Hit Fwd Refs

End of Result Set

☐ Generate Collection Print

L4: Entry 1 of 1 File: USPT Dec 16, 2003

US-PAT-NO: 6665807
DOCUMENT-IDENTIFIER: US 6665807 B1

TITLE: Information processing apparatus

DATE-ISSUED: December 16, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kondo; Nobukazu	Ebina			JP
Noguchi; Koki	Tokyo			JP
Kawasaki; Ikuya	Kodaira			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 09/ 389228 [PALM]
DATE FILED: September 3, 1999

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATION This application relates to U.S. Patent Application Serial No. to be assigned based on Japanese Patent Application No. 10-250710 filed Sep. 4, 1998 entitled "INFORMATION PROCESSING APPARATUS" by N. Kondo et al., the disclosure of which is incorporated herein by reference.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	10-250710	September 4, 1998
JP	11-228241	August 12, 1999

INT-CL: [07] G06 F 1/12

US-CL-ISSUED: 713/400; 370/94, 371/471, 714/731
US-CL-CURRENT: 713/400; 370/236, 714/731

FIELD-OF-SEARCH: 370/94, 714/731, 371/47.1, 713/400

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4654654	March 1987	Butler et al.	340/825.5
☐	4873703	October 1989	Crandall et al.	375/371
☐	4965793	October 1990	Polzin et al.	370/94
☐	5029124	July 1991	Leahy et al.	
☐	5428753	June 1995	Kondo et al.	
☐	5768529	June 1998	Nikel et al.	
☐	5915130	June 1999	Kim	395/888
☐	5919254	July 1999	Pawlowski et al.	
☐	5963609	October 1999	Huang	375/377
☐	6055285	April 2000	Alston	375/372
☐	6145039	November 2000	Ajanovic et al.	
☐	6336159	January 2002	MacWilliams et al.	
☐	6381293	April 2002	Lee et al.	375/377

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
403058263	July 1990	JP	

ART-UNIT: 2185

PRIMARY-EXAMINER: Lee; Thomas

ASSISTANT-EXAMINER: Patel; N C

ATTY-AGENT-FIRM: Antonelli, Terry, Stout & Kraus, LLP

ABSTRACT:

A circuit includes a transmission function of transmitting data together with a source clock synchronized to the data to another module, a reception circuit for receiving the data outputted by the module and a source clock synchronized to the data, and a synchronization circuit for connecting the circuit having a transmission function to the reception circuit are formed on a single-chip integrated circuit. Even if the module connected to the bus is changed, i.e., even if the operation clock frequency of the module of the other party is changed, other modules can be used as they are without making any change. The cost needed at the time of system construction can thus be reduced. Furthermore, as for the aspect of performance, only one synchronization circuit is needed. The increase of latency caused by synchronization can also be suppressed to the minimum.

16 Claims, 26 Drawing figures

First Hit Fwd Refs

End of Result Set

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L3: Entry 1 of 1 File: USPT Oct 19, 1999

DOCUMENT-IDENTIFIER: US 5970069 A
TITLE: Single chip remote access processor

Detailed Description Text (7):
In alternative embodiments, remote access processor 34 can be located within PC 52 or portable PC 53 to provide LAN and WAN port expansion, which allows connectivity to a diverse set of network interfaces. In FIG. 2b, remote access processor 34 is implemented within an edge router 63. LAN interface 36 is coupled to a plurality of PCs 52a-52c over Ethernet network 50, which allows connectivity to WAN 54 over a variety of SWAN interfaces 40, 42 and 44. Edge router 63 can be located in a stand-alone box, in network server 30 or in any one of the PCs 52a-52c.

Detailed Description Text (8):
FIG. 3 is a block diagram of remote access processor 34. Remote access processor 34 is implemented on a single integrated circuit chip having a plurality of inputs and outputs. In one embodiment, the integrated circuit chip is manufactured with a 3.3 volt, 0.35 micron CMOS fabrication technology and is packaged within a 256 position plastic ball grid array having nominal dimensions of 27 mm.times.27 mm.times.2.1 mm. The communication interfaces include LAN interface 36, PCI interface 38 and SWAN interfaces 40, 42a, 42b and 44. SWAN interface 40 is a multi-protocol SWAN interface. SWAN interfaces 42a and 42b are time division multiplexer (TDM) serial interfaces for supporting two ISDN-BRI networks. SWAN interface 44 is a V.34 coder-decoder (CODEC) interface for coupling to a V.34 CODEC modem. The remaining inputs and outputs of remote access processor 34 include serial peripheral interface (SPI) 55, reference clock input 56, real time clock (RTC) input 57, battery back-up input 58, UART compatible serial I/O port 60, 40 Mhz clock input 62, boundary scan test I/O 64, 32-bit local memory interface 66 and general purpose interrupt/control I/O 70.

Detailed Description Text (16):
Memory controller 110 is coupled between local memory interface 66 and internal transfer bus 86. Memory controller 110 is also coupled to DMA controller and bridge circuit 112. Memory controller 110 is an integrated memory controller for supporting various local peripheral memory devices, such as a 32-bit SDRAM or an 8-bit PROM, which may be coupled to local memory interface 66. DMA controller and bridge circuit 112 is coupled between memory controller 110 and PCI interface circuit 114, and has data, address and control buses coupled to internal transfer bus 86. Circuit 112 transfers data packets between PCI interface 114 and local memory, through memory controller 110 and under the control of CPU 90. PCI interface circuit 114 is coupled between PCI interface 38 and internal transfer bus 86. PCI interface 114 is a 33 Mhz, 32-bit (3.3 Volt/5.0 Volt) interface which allows connection to external devices such as a host processor, additional LAN and WAN ports, multiple remote access processors, or network servers, for example. Finally, general purpose interrupt and control circuit 116 is coupled between interrupt and control interface 70 and internal transfer bus 86. In one embodiment, circuit 116 includes twelve programmable, bidirectional pins for serving additional interrupt inputs or control outputs.

Detailed Description Text (28):
When serial data is received at V.34 Codec interface 44, the data represents a sampling of the analog signal transmitted over a public switched telephone network. The sampling is performed by an external V.34 Codec (not shown) coupled to V.34 Codec interface 44. As in the case where serial data is received at one of the LAN or WAN ports DMA controller 82 collects the serial data and stores the data in local memory, through memory controller 110. Once the data samples have been stored in local memory, CPU 90 retrieves the data samples and demodulates the samples into digital data packets by performing a digital filter and data pump function through the V.34 digital signal processing algorithm. CPU 90 then stores the data packets back into local memory through memory controller 110, and notifies the routing software executed by CPU 90 to look for the packets in local memory. The routing software then retrieves the packets from local memory and determines their destination, as discussed above.

Detailed Description Text (31):
FIG. 5 is a block diagram of an application of remote access processor 34 according to the configuration shown in FIG. 4c. PCI interface 38 is coupled to PCI bus 150, which is coupled to host processor 152. LAN interface 36 is coupled to an Ethernet physical layer device 154, such as a DP83840VCE PHY device which is available from National Semiconductor Corporation. Isolation transformer circuit 156 is coupled between Ethernet physical layer device 154 and LAN network 158 for communication over LAN network 158. Local memory interface 66 is coupled to local memory bus 160, which is coupled to DRAM 162, flash ROM 164, DS-1/E1 Frame Relay framer 166 and Siemens 2186 ISDN transceiver 168. DRAM 162 and flash ROM 164 form the local memory for storing the software algorithms executed by remote access processor 34 and for storing data packets received from the various communications ports of remote access processor 34.

Detailed Description Text (32):
TDM serial interface port 42a is coupled to ISDN transceiver 168. ISDN front end circuit 170 is coupled between ISDN transceiver 168 and ISDN network 172. Similarly, multi-protocol SWAN interface 40 is coupled to framer 166. A DS-1 CSU/E1 isolation transformer circuit 176 is coupled between framer 166 and SWAN network 178. Flash ROM 164 provides 8-bits of instruction data over local memory bus 160. Remote access processor 34 controls the operation of ISDN transceiver 168 and framer 166 using 8-bit bus 174. In an alternative embodiment, in which a Motorola ISDN transceiver is used, SPI interface 55 provides control for the transceiver.

Detailed Description Text (157):
The RAP's Central Processing Unit (CPU 90) is based upon LSI Logic Corporation's CW4011 MiniRISC.TM. high performance processor core. CW4011 is the G10 implementation of the LSI Logic CW4010 superscalar MIPS processor. A block diagram of CPU 90 is shown in FIG. 9. CPU 90 interfaces to RAP logic via two interfaces. The SC-bus 220 is a 32-bit bus for accessing PCI, Local Memory and RAP internal registers. The On Chip Access (OCA) 222 bus provides high speed access to the SRAM 84 used as shared memory with the DMA Controller 82. In addition to the CW4011 core, CPU 90 provides: direct-mapped or two way set associative instruction cache, direct-mapped or two-way set associative data cache, a writeback buffer for writeback cache mode, reset control and address translation hardware. The RAP Chip and CW4011 core are configured such that all data structures are big endian.

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L3: Entry 1 of 1 File: USPT Oct 19, 1999

US-PAT-NO: 5970069
DOCUMENT-IDENTIFIER: US 5970069 A

TITLE: Single chip remote access processor

DATE-ISSUED: October 19, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kumar; Shailendra	San Jose	CA		
Sonnek; Christopher D.	North St. Paul	MN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
LSI Logic Corporation	Milpitas	CA			02

APPL-NO: 08/ 840575 [PALM]
DATE FILED: April 21, 1997

INT-CL: [06] H04 L 12/28, H04 J 3/16

US-CL-ISSUED: 370/402; 370/401, 370/466
US-CL-CURRENT: 370/402; 370/401, 370/466

FIELD-OF-SEARCH: 370/351, 370/355, 370/357, 370/360, 370/389, 370/401, 370/402, 370/465, 370/466, 370/463, 370/467

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5610910	March 1997	Focsaneanu	370/401
☐	5640399	June 1997	Rostoker	370/402

ART-UNIT: 272

PRIMARY-EXAMINER: Patel; Ajit

ASSISTANT-EXAMINER: Pizarro; Ricardo M.

ATTY-AGENT-FIRM: Westman, Champlin & Kelly, P.A.

ABSTRACT:

A single chip integrated remote access processor circuit has a plurality of communication interface units, including a local area network (LAN) interface unit, a first multi-protocol serial wide area network (SWAN) interface unit, a telephony coder-decoder interface unit and a peripheral component interface (PCI) unit. A data routing control circuit is coupled to the plurality of communication interface units for controlling data transfer between the interface units.

18 Claims, 185 Drawing figures

First Hit Fwd Refs

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L3: Entry 40 of 52 File: USPT Sep 17, 1996

DOCUMENT-IDENTIFIER: US 5556107 A
TITLE: Computer game apparatus for providing independent audio in multiple player game systems

Detailed Description Text (23):
In operation, a program executed by the CPU 200 utilizes sound data stored in the mass storage device 204 to generate unique independent sounds to each player as provided by the application. The digital input device controller 210 handles the two-way communication of data and sound between the game controllers 214, 216, 218 and 220. Illustrated in FIG. 5 is a representative game controller 214 which includes a serial bus interface circuit 240 coupled over line 242 to the high speed bus 212. A microcontroller 242 is coupled to the serial bus interface 240. The microcontroller 242 may comprise a general purpose microprocessor, or alternatively, may comprise a custom microcontroller. A DAC 246 is coupled to the microcontroller 242 and to headphones 248. Sound data is provided from the sound synthesizer circuit 208 through the digital input device controller 210 and coupled over the high speed bus 212 to the serial bus interface 240. The microcontroller 242 further couples this digitized audio to the DAC 246 which converts the digitized audio into analog signals. A player utilizing the game controller 214 will then hear independent audio intended for, and directed to, that player using the headphones 248.

First Hit Fwd Refs

Generate Collection Print

L3: Entry 34 of 52 File: USPT Sep 1, 1998

DOCUMENT-IDENTIFIER: US 5802069 A
TITLE: Implementing mass storage device functions using host processor memory

Detailed Description Text (2):
The provisional applications incorporated herein by reference provide detailed descriptions of mass storage devices according to preferred embodiments of the present invention. The preferred mass storage devices of the present invention are designed to operate in PC systems that have a high-speed bus called the Intel.RTM. Serial Express.TM. (SE) bus, which is also described in detail in the teachings of the provisional applications. The SE bus provides mass storage devices with direct memory access to host memory.

First Hit Fwd Refs

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L3: Entry 34 of 52 File: USPT Sep 1, 1998

US-PAT-NO: 5802069
DOCUMENT-IDENTIFIER: US 5802069 A

TITLE: Implementing mass storage device functions using host processor memory

DATE-ISSUED: September 1, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Coulson; Richard	Portland	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 627939 [PALM]
DATE FILED: March 28, 1996

INT-CL: [06] G06 F 11/00

US-CL-ISSUED: 371/21.1; 395/182.06
US-CL-CURRENT: 714/718; 714/8

FIELD-OF-SEARCH: 371/21.1, 395/182.03, 395/182.05, 395/182.06, 395/183.16, 395/183.18, 364/238.3, 364/238.4, 364/236.2, 364/239

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5257367	October 1993	Goodlander et al.	364/236.2

OTHER PUBLICATIONS

"P1394 IEEE Draft Standard for a High Performance Serial Bus," by IEEE, P1394, D8.Ov2, Jul. 1995, DS3285, pp. 1-384.

ART-UNIT: 243

PRIMARY-EXAMINER: Canney; Vincent P.

ATTY-AGENT-FIRM: Duane, Morris & Heckscher LLP

ABSTRACT:

A computer system comprises a host processor, host memory, and a mass storage device interconnected via a high-speed data bus. An operating system and a driver for the mass storage device are implemented on the host processor. The mass storage device is capable of being connected to the computer system via the data bus, such that a portion of the host memory is allocated for use by the mass storage device; the mass storage device uses the host memory portion for one or more particular mass storage device operations; and the operating system and the driver are unaware of how the mass storage device uses the host memory portion. In a preferred embodiment, the mass storage device requests and the host processor allocates a portion of host memory for exclusive use by the mass storage device to perform such functions as predictive failure analysis, maintenance of deallocated sector lists, and data prefetching.

39 Claims, 5 Drawing figures

L3: Entry 33 of 52 File: USPT Sep 15, 1998

DOCUMENT-IDENTIFIER: US 5809337 A
TITLE: Mass storage devices utilizing high speed serial communications

Detailed Description Text (7):
The low latency, high bandwidth and DMA capabilities of high-speed serial bus 25 further aid real-time processing by microprocessor 22 of computer 20 of the digital signals being transmitted between mass storage device 30 and computer 20. This feature eliminates a need for an on-board, embedded processor for digital signal processing in mass storage device 30, as was known in conventional mass storage devices, such as processor 13 in mass storage device 10 of FIG. 1. Conventional mass storage devices, such as mass storage device 10 coupled to computer 20 through conventional bus 15, require on-board, closely coupled processor, such as processors 13, to process the digital signals in a timely fashion. Since high-speed bus 25 aids real-time signal transmission between mass storage device 30 and computer 20, digital signals may be processed by microprocessor 22 of computer 20 as if it were a closely-coupled processor on-board mass storage device 30. Therefore, digital signals being written to storage medium 31 can be processed by microprocessor 22 of computer 30 first and transmitted over bus 25 in real-time for storage on storage medium 31. Similarly, digital signals being read from storage medium 31 of mass storage device 30 can be sent in real-time over low latency, high-bandwidth bus 25 for real-time processing by microprocessor 22 of computer 20.

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L3: Entry 33 of 52 File: USPT Sep 15, 1998

US-PAT-NO: 5809337
DOCUMENT-IDENTIFIER: US 5809337 A

TITLE: Mass storage devices utilizing high speed serial communications

DATE-ISSUED: September 15, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hannah; Eric C.	Pebble Beach	CA		
Hauck; Jerrold V.	Fremont	CA		
Coulson; Richard L.	Portland	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 623759 [PALM]
DATE FILED: March 29, 1996

PARENT-CASE:
CROSS-REFERENCES TO RELATED APPLICATIONS This non-provisional U.S. national application, filed under 35 U.S.C. .sctn.111(a) claims, under 35 U.S.C. .sctn.119 (e)(1), the benefit of the filing date of provisional U.S. applications Nos. 60/006,431, filed under 35 U.S.C. .sctn.111(b) on Nov. 10, 1995; 60/011,320, filed under 35 U.S.C. .sctn.111(b) on Feb. 8, 1996; and 60/013,302, filed under 35 U.S.C. .sctn.111(b) on Mar. 8, 1996 , the teachings of all three being incorporated herein by reference.

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/853; 395/872, 395/892, 395/878, 395/888, 395/885, 395/250, 395/880, 711/100
US-CL-CURRENT: 710/33; 710/52, 710/58, 710/60, 710/65, 710/68, 710/72, 711/100

FIELD-OF-SEARCH: 395/250, 395/892, 395/208, 395/883-885, 395/872-879, 395/880-889, 711/106

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL

h e b b g e e e f c e bh e ge

☐	4124888	November 1978	Washbura	395/828
☐	4344132	August 1982	Dixon et al.	395/250
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☐	5594743	January 1997	Park	371/40.1
☐	5621820	April 1997	Rynderman et al.	382/239

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IEEE Draft Standard for a High Performance Serial Bus, P1394, D8.0v2, Jul. 1995, DS3285. Institute of Electrical and Electronics Engineers, Inc.

ART-UNIT: 272

PRIMARY-EXAMINER: Shin; Christopher B.

ATTY-AGENT-FIRM: Duane, Morris & Heckscher LLP

ABSTRACT:

A mass storage device having a storage medium on which digital signals can be stored. The mass storage device is coupleable to a computer through a high-speed serial bus. The high-speed serial bus has a latency and a signal transmission rate sufficient to enable transmission of digital signals between the mass storage device and the computer without interim storage of the digital signals in a buffer inside the mass storage device. The computer has a processor capable of processing the digital signals and the digital signals may be transmitted between the mass storage device and the computer without processing of the digital signals by a processor in the mass storage device.

16 Claims, 2 Drawing figures

L3: Entry 1 of 1 File: USPT Oct 19, 1999

DOCUMENT-IDENTIFIER: US 5970069 A
TITLE: Single chip remote access processor

Detailed Description Text (8):
FIG. 3 is a block diagram of remote access processor 34. Remote access processor 34 is implemented on a single integrated circuit chip having a plurality of inputs and outputs. In one embodiment, the integrated circuit chip is manufactured with a 3.3 volt, 0.35 micron CMOS fabrication technology and is packaged within a 256 position plastic ball grid array having nominal dimensions of 27 mm.times.27 mm.times.2.1 mm. The communication interfaces include LAN interface 36, PCI interface 38 and SWAN interfaces 40, 42a, 42b and 44. SWAN interface 40 is a multi-protocol SWAN interface. SWAN interfaces 42a and 42b are time division multiplexer (TDM) serial interfaces for supporting two ISDN-BRI networks. SWAN interface 44 is a V.34 coder-decoder (CODEC) interface for coupling to a V.34 CODEC modem. The remaining inputs and outputs of remote access processor 34 include serial peripheral interface (SPI) 55, reference clock input 56, real time clock (RTC) input 57, battery back-up input 58, UART compatible serial I/O port 60, 40 Mhz clock input 62, boundary scan test I/O 64, 32-bit local memory interface 66 and general purpose interrupt/control I/O 70.